Transmission Line Modelling for Multi-Gigabit Serial Interfaces

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Abstract
Modern Computer systems increasingly use high-speed multi-gigabit/second (GB/s) serial printed circuit board (PCB) interconnects in order to transfer data between components, both on board, to daughter cards and across backplanes. As the transmission speeds increase it is becoming increasingly more difficult in terms of time and money, to measure the integrity of the received signals and engineers are reliant on simulation to ensure low bit error rate (BER) communication. Transmission line losses are one of major limiting factor in terms of distance capability and speed of operation for these modern high speed serial communication systems. Therefore the accurate modelling of losses in PCBs has recently become an area of intense investigation.

Dielectric models have been formulated, containing the physics of the dielectric loss mechanism that predict the experimentally observed behaviour of the woven glass and resin construction of the composite laminate. At the frequencies excited in high speed digital serial links, the current flows predominantly at the surface of the conductor due to the skin effect and is thus strongly affected by any atomic scale surface roughness. Several new models have been proposed that deal with the additional losses caused by surface roughness, as the frequencies of the serial interconnect increase.

Simulation work has been carried out for multi-GB/s interconnects with the new aforementioned conductor loss models demonstrating improvements in accuracy and better agreement with experimental data.
Introduction

Modern Computer systems increasingly use high-speed multi-gigabit/second (GB/s) serial interconnects in order to transfer data between components, both on board, to daughter cards and across backplanes. Examples of such interfaces as Peripheral Component Interconnect Express (PCI-E), Serial Advanced Technology Attachment (SATA) and Hyper-transport, for reasons of performance these interfaces are invariably implemented as differential signals [Derickson, Muller, 2008].

![Diagram of Typical Desktop Computer Architecture Based on High Speed Serial Interconnects.](image)

Two example applications of high speed serial interconnects are shown in Figure 1 and Figure 2. Figure 1 shows a typical desktop personal computer architecture with three high speed serial interconnect standards, PCI-E, SATA and Universal serial bus (USB). An example of an embedded computer architecture is shown in Figure 2, the high speed serial interconnect is implemented in PCI Express but other standards such as RapidIO and Ethernet are also commonly used. Embedded computer architectures are those that are typically used in systems that perform one task or a limited set of tasks and is part of an overall solution. A typical commercial example of an embedded system is an engine management system in a car, which has powerful processing, a large number of input sensors and output actuators.

The first generations of these standards operated in region of 1.5 - 2.5 GB/s, second generation implementations operate in the 3 -5 GB/s and more recently third generations have been proposed operating at even higher bit rates [Derickson, Muller, 2008].
Most of the interconnect standards have been developed out of the low cost computing environment such as personal computing, business computing and the like. In these markets cost is a prime factor and manufacturers strive to engineer the cheapest possible solution. For this reason manufacturers typically try to use the cheapest dielectric material possible for the printed circuit board fabrication; in general this will mean an FR-4 based material. FR-4 is a common name for a range of materials made from a combination of flame retardant epoxy and woven glass and is defined by IPC-4101 [IPC, 1997] and has a mature process technology.

Although improved FR-4 materials are available with low dielectric losses in general there is a cost penalty which the producers of volume electronics products are not willing to pay. Even in higher end products there is reluctance to move to these ‘exotic’ dielectrics as they can behave mechanically differently than perceived ‘standard’ FR-4 formulations.

Why Are Accurate Simulations Necessary?

Verification by measurement of multi-gigabit/second serial interfaces is becoming increasingly difficult. Measurement in the time domain using oscilloscopes can lead misleading results due to the non-ideal probing positions caused by signal reflections. Measurements in the frequency domain require expensive instrumentation and measurements fixtures. It is therefore becoming necessary to rely on simulation techniques to ensure that the interface will operate to the low bit error rates required with adequate margins. The simulations shown in Figure 3 were carried out in Agilent Technologies ADS and show eye diagram measurements of a simplified channel both at the package balls and at the silicon receiver. In the simulations a generic behavioural IBIS-AMI model (supplied as part of the ADS tool) of a second generation PCI-E transceiver was used. It is common practice for Gb/s transceivers to be packaged in ball grid arrays [Amkor, 2011] to allow controlled impedance transitions between the silicon die, package and PCB. The ADS simulation uses a generic four port package model; the driver launches a 1.2 $V_{pp}$ differential signal with rise/fall times of 30 ps. Without built-in eye measurement facilities on the silicon die (which is expensive in silicon area), the left hand eye is typical of that which might be measured with
an oscilloscope at the BGA balls on the rear of the PCB. While it is possible to de-embed the measurements at the balls to give an equivalent eye at the die, it is too late to fix the design once it has been physically built. Accurate simulations allow the designer to explore the design space and develop a product that is robust before assembly.

![Figure 3 Simulated Eye Diagrams for 5Gb/s Serial interconnect at the Balls of the BGA (left) and at the receiver die (right) for a PCI-E transceiver modelled using a generic behavioural IBIS-AMI model.](image)

The physical distance that can be achieved between devices in an electronic system using Gb/s serial interfaces is limited by the electrical losses; noise and timing jitter within the system. The electrical losses in the transmission line stem from two main sources, namely conductor and dielectric loss [Hall, Heck, 2009].

The conductor loss includes both resistive direct current (DC) loss that occurs because of the finite conductivity of copper and frequency dependent alternating current (AC) losses caused by the ‘skin effect’ and surface roughness. In Figure 4, which shows analytical models [Bogatin, 2004] of a 8 mil microstrip transmission line attenuation versus frequency for the dielectric and conductor loss contributions, the slope of conductor loss curve due to skin effect is 0.5 when plotted on a log-log scale. This indicates that skin depth losses are related to the square root of frequency:

\[ \alpha_c \propto \sqrt{f} \]  

\[ \text{Eq. 1} \]

![Figure 4 Example of Transmission Line Loss Contributors for an 8 mil Micro-stripline. The blue curve shows the frequency dependence of the dielectric loss while the red curve shows the frequency dependence for the conductor loss. The green curve is for the total attenuation versus frequency.](image)
The conductor losses shown in Figure 4 are based on the simple Hammerstad and Jensen model [Hammerstad, Jensen, 1980], which underestimate the losses in the channel. Any channel simulations using the simple Hammerstad and Jensen surface roughness model will give overly optimistic bit error rate or channel length predictions.

Dielectric (tan delta) losses are caused by the polarisation of the molecules within the dielectric. In Figure 4 it can be seen that the dielectric loss dominates at higher frequencies. On the log-log scale of the figure, the dielectric loss has a slope of one, indicating that the dielectric loss has a square dependency on frequency \( f \), that is:

\[
\alpha_d \propto f^2
\]

The dielectric behaviour of typical printed circuit board materials used in digital electronics can be modelled using the wideband Djordjevic model [Djordjevic, Sarkar et al, 2001]. [Huray, Pytel, 2008] compared the attenuation loss of a transmission line modelled with a wideband Debye dielectric model combined with the Hammerstad-Jensen surface roughness correction factor with a measured sample. This work showed a significant difference between the simulated and measured results above 5 GHz due to the limitation of the Hammerstad-Jensen correction.

**Conductor Surface Roughness Models**

In order to understand why the conductor loss is greater than predicted by the Hammerstad-Jensen model is it necessary to appreciate how printed circuit boards are fabricated. The copper foils are produced by electro-deposition and the process is shown in Figure 5. The copper foil is initially deposited on a drum and the resulting copper foils have a smooth (drum) side and a rougher side, known as shiny and matte sides respectively. After the initial electro-deposition additional processing stages are applied which prevent oxidisation and increase the surface roughness. Typically Electrodeposited cooper have a root mean square (RMS) surface roughness of between 1.5 and 3.0 \( \mu m \) before additional treatments by the PCB fabricator. The RMS surface roughness refers to the standard deviation for the variation in height of the roughness.

In the PCB fabrication process it is important that copper has sufficient roughness to allow the adhesion of the epoxy glass (or other dielectric materials). If the surface is too smooth then the assembly may ‘de-laminate’ either during the fabrication process or when components are soldered to the PCB. Typical high density PCBs have between 10 and 30 layers and are 1 - 3 mm in thickness.
As the frequency of signals increases, the signal currents in the conductor do not penetrate the metal surface further than a depth of $\delta$ because it has finite conductivity. This is known as the skin effect and is defined from the conductivity $\sigma$, the angular frequency $\omega$ and the magnetic permeability $\mu$ as:

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}} \text{ Metres} \quad \text{Eq. 3}$$

Figure 6 shows the skin depth of copper at different frequencies compared to a typical ‘rough copper’ which has nodules with an RMS height of 5.8 $\mu$m. Even at frequencies as low as 1 GHz the signal fails to penetrate the surface roughness to the ‘smooth’ copper underneath.

Figure 6 Microscopic View of Surface Roughness [Hall, Heck, 2009]. The skin depth ($\delta$) at frequencies of 1GHz, 10GHz and 100GHz are drawn to scale as vertical lines for comparison purposes.

As the frequency of a signal increases due to the skin effect the current tends to flow only on the metal surface in a layer of thickness $\delta$ which allows a surface resistivity to be defined. Figure 7 shows the current flowing in a microstripline transmission line made from smooth metal at a frequency where the skin depth is well established. The equivalent “AC” resistance can be calculated from the conductor width ($W$), skin depth ($\delta$), conductivity ($\sigma$) and the conductor length ($l$) from:

$$R_{ac} = \frac{l}{w\delta\sigma} \text{ Ohms} \quad \text{Eq. 4}$$

Figure 7 Current Density Profile in a Microstripline Transmission Line. Note that the current in the top conductor is significant only within the skin depth.

Assuming unit length, Eq. 4 can be re-written in the form:

$$R_{ac} = R_s\sqrt{f} \text{ Ohms} \quad \text{Eq. 5}$$
Where:

\[ R_s = \frac{\omega \mu}{2\sigma} \text{Ohms/square} \quad \text{Eq. 6} \]

\( R_s \) is called the surface resistivity and assumes a smooth surface and is expressed in ohms per square unit area.

**Hammerstad Jensen Model**

The surface resistivity expressed by Eq. 6 assumes a smooth surface however from the roughness profile shown in Figure 6 and at the frequencies of interest for GB/s serial interfaces the current is flowing in the tooth profile. [Samuel P. Morgan, 1949], proposed a model that was based on the grooved profiles shown in Figure 8. Note that some authors show the current flowing up and down the tooth profile; this is not physically possible because it would mean that the propagation time of a signal on a trace would increase. Increases in signal flight time on smooth and rough coppers are not observed in measurement and therefore models based on such a formulation would result in a non-physical model.

![Figure 8 The Two Surface Roughness Models Proposed by [Samuel P. Morgan, 1949]: One Rectangular drawn on the left hand side and the Other Triangular drawn on the right hand side.](image)

Hammerstad and Jensen used the work of Morgan and the RMS surface roughness \( (H_{RMS}) \) to drive an analytical model of the AC resistance due to surface roughness.

\[ K_{HJ} = 1 + \frac{\pi}{2} \arctan \left[ 1.4 \left( \frac{H_{RMS}}{\delta} \right)^2 \right] \quad \text{Eq. 7} \]

The Hammerstad-Jensen is applied as a correction factor to the surface roughness so that the AC resistance becomes:

\[ R_{ac} = K_{HJ} R_s \sqrt{f} \text{ Ohms} \quad \text{Eq. 8} \]

The correlation of the Hammerstad–Jensen correction factor in relation to two copper roughness profiles was investigated in [Hall, Heck, 2009]. They found for smooth copper \( (H_{rms} = 1.2 \ \mu m) \) the predicted transmission line losses correlated well up to around 15 GHz. For rougher coppers surface finishes \( (H_{rms} = 5.8 \ \mu m) \) the model correlated well up to approximately 5 GHz.

**The Hall Model**

The Hall model models the surface roughness as an array hemispheroidal ‘bosses’ on a flat surface. The dimensions of the bosses are approximated from measurements using optical profilimeters, which measure the RMS distance between the peaks and the height of the peaks (see Figure 9). The electromagnetic wave propagates as a plane wave where it is reflected from and absorbed by the bosses. The Hall model has increased losses and is physically more realistic than the Hammerstad Jensen model.
The hemispherical bosses are placed on square bases whose dimensions are arranged to be those of the distance between the peaks (see Figure 10). The radius of the bosses themselves, are calculated such that the volume of the boss is equivalent to that of the tooth based on the RMS height and the tooth base. Just using the base width was shown to underestimate the conduction losses.

\begin{equation}
K_{Hall} = 1 \text{ when } K_s \leq 1 \text{ and } K_{Hall} = K_s \text{ when } K_s > 1.
\end{equation}

The correction factor is effectively the ratio of the power loss from the hemispheroid and the power loss that would have occurred from a flat surface and is calculated from:

\begin{equation}
K_S = \frac{\text{Re}\left[\eta^3 \pi / 4k^2 (\alpha(1) + \beta(1)) \right] \mu \omega \delta (A_{Tile} - A_{base})}{\mu \omega \delta (A_{Tile})}
\end{equation}

A plane electromagnetic wave hitting the hemispheroid will be partly scattered and partly absorbed if the hemispheroid is made from a ‘good’ conductor. The first term in the numerator represents the power loss in the hemispheroid. The equivalent boss radius is used in the calculation of the scattering and absorption coefficients. As the hemispheroid is not the same size as the ‘tile’ the second term in the numerator represents the loss from remaining surface area (flat part). The scattering (\(\alpha\)) and absorption (\(\beta\)) coefficients can be calculated and their sum would represent the total power of an Electromagnetic wave impinging on the hemispheroid. The denominator represents the power absorbed by a flat plane, i.e. the skin depth power loss due to finite conductance of the smooth copper. The correction factor is applied in a similar way to that of the Hammerstad-Jensen correction as a modification of the surface resistivity such that: -
Note that the scattering and absorption coefficients are in fact summations. It has been found that only the first term is required for sufficient accuracy up to 50 GHz.

When the Hall surface roughness correction factor is used in conjunction with a wide band dielectric model it has been observed, [Hall, Pytel, et al, 2007] that the Hall model slightly overestimates the conductor losses in the 1-20 GHz range and then underestimates the losses above 20 GHz.

**The Huray Model**

The Huray model was formulated to address the limitations of the previous models. Huray observed that the surface roughness ‘nODULES’ looked like a collection of ‘snowballs’ of various sizes. However a model based on non-uniform spheres is difficult to create and so a uniform ball size was assumed as a mathematical expediency.

Again a hemispheroid is chosen to represent the surface roughness structure and the number of uniform spheres equal to the volume of the hemispheroid calculated. Again the parameters for the hemispheroid are derived from the RMS values measured by the optical profilers. As in the Hall model, the Huray correction factor is calculated as the ratio of the power losses for a flat surface and the power loss of the spheres. In the Huray model the surface roughness is broken up into ‘tiles’ the area of each ‘tile’ $A_{tile}$ is based on the distance between the peaks as measured using an optical profilometer.

$$K_{Huray} = \left[\frac{\mu_0 \omega \delta / A}{(\mu_0 \omega / \delta A)} A_{Tile} + \sum_{n=1}^{N} Re\left\{\frac{1}{2\pi/\kappa^2}\left(\alpha(1) + \beta(1)\right)\right\}\right]$$

The scattering ($\alpha$) and absorption ($\beta$) coefficients are calculated for each of the $N$ spheres making up the snowball. The Huray model can be applied to both smooth (1 - 2 $\mu$m RMS roughness) and rough coppers (4 - 6 $\mu$m RMS roughness) without modification. Again $K_{Huray}$ is applied as a modification to the surface resistance:

$$R_{ac} = K_{Huray} R_s \sqrt{f} \text{ Ohms}$$

It was observed [Hall, Heck, 2009] that when the insertion loss was modelled with a wideband dielectric model and the Huray surface roughness correction factor, there was close agreement between the theoretical and experimental results.
Comparison of the Surface Roughness Models

Figure 12 shows the three surface roughness correction factors plotted against frequency up to 20 GHz for an RMS surface roughness of 5.8 μm. The RMS surface roughness of 5.8 μm is typical of a rough copper after additional treatment by the PCB vendor.

Above 3 GHz the Hammerstad-Jensen Model saturates at a value of 2, accounting for why the model underestimates the conductor losses as the frequency increases for rough coppers. For smooth copper foils the saturation point is shifted up in frequency. The Hall Model is also shown to overestimate the conductor losses above 500 MHz or so with the 5.8 μm of surface roughness.

Figure 12 Comparison of the Hammerstad-Jensen, Hall and Huray Surface Roughness Correction Factors for an RMS surface roughness of 5.8 μm.

Figure 13 shows the total loss of a 50 Ohm stripline versus frequency. The total loss is defined as the sum of the conductor loss \( \alpha_C \) and dielectric loss \( \alpha_D \) as:

\[
\alpha_{Total} = \alpha_D + \alpha_C \quad \text{Eq. 13}
\]

Closed form expressions for the dielectric losses (\( \alpha_D \)) and conductor losses (\( \alpha_C \)) for stripline transmission lines can be found in [Cohn, 1955] and [Collins, 1992]. The physical dimensions of the transmission line used are typical of those encountered in a modern PCB. The track width is 90 μm, and the dielectric thickness is 230 μm. The tracks are 18 μm thick, common when 1/2 oz/ft² copper is used. The dielectric is medium loss material with a Relative Permittivity of 3.9 and loss tangent of 0.007 at 1GHz. A wideband Djordjevic-Sarkar [Djordjevic, Sarkar et al, 2001] model has been used to in all cases to model the dielectric losses. The copper has a RMS surface roughness of 5.8 μm and the RMS distance between the peaks is 9.4 μm. At 10 Ghz The Hammerstad-Jensen model underestimates the received power by 3 dB/m compared with the Huray model. The Hall model over estimates the losses by approximately 4dB/m compared with the Huray model.

A salient point is that if the copper losses are not modelled correctly, then non causal transmission line models can result. Non-causal models can cause time domain simulators to fail to converge and give erroneous results.
Conclusion

In modern computer systems high speed serial communications technologies such as PCI and PCI-E have, to a greater extent, taken the place of the wide parallel bus architectures. The move away from the parallel bus architectures was in part due to the increasing difficulty of maintaining the required timing relationships between the clock and data, but also due to the impracticalities of the PCB routing density required. High speed serial communications became the obvious choice but have presented a new set of engineering challenges to overcome. The work presented in this paper show some of the engineering considerations necessary, in terms of the requirement for introducing advanced physics models of the dielectric and PCB track surface roughness, in order to successfully implement high speed serial interconnects in the multi-GB/s era. Recent work in the field [Hall, Heck, 2009], [Hall, Pytel, et al, 2007] and [Huray, 2010] have shown that conductor losses have a greater effect than previously predicted by [Hammerstad, Jensen, 1980]. This paper has given an overview of how these models are constructed and has compared the performance of these models with measured data.
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